REMARKS

Claims 1-6 and 19-29 are all the claims presently pending in the application. Claims 7-18 have been canceled. Claim 1 has been amended to more particularly define the invention. Claims 19-29 have been added.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicant gratefully acknowledges the Examiner's indication that claims 2-6 would be allowable if rewritten in independent form. However, Applicant respectfully submits that all of the claims are allowable.

Claim 1 stands rejected under 35 U.S.C. 102(e) as being allegedly unpatentable over Ramanath et al. (U. S. Patent Pub. No. 2002/0079487).

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

An exemplary aspect of the claimed invention (e.g., as recited in claim 1) is directed to a circuit including a template including first and second layers, a semiconductor material self-assembled on a side of the first layer of the template, and a self-assembled connection between the semiconductor material and the second layer of the template.

Convention circuits are formed using lithographic techniques. However, this requires many expensive processing steps (Application at [0005]).

The claimed circuit, on the other hand, includes a template including first and second layers, a semiconductor material self-assembled on a side of the first layer of the template, and a self-assembled connection between the semiconductor material and the second layer of the template (Application at Figure 2; [0036]-[0037]). The claimed circuit may be formed without the expensive lithographic techniques required by conventional circuits.

II. THE ALLEGED PRIOR ART REFERENCE

The Examiner alleges that Ramanath teaches the invention of claim 1. Applicant submits, however, that Ramanath does not teach or suggest each and every feature of the claimed invention.

In particular, Ramanath does not teach or suggest a circuit including "*a template comprising first and second layers; a semiconductor material self-assembled on a side of said first layer of said template; and a self-assembled connection between the semiconductor material and the second layer of said template*", as recited in claim 1. As noted above, the claimed circuit may be formed without the expensive lithographic techniques required by conventional circuits.

Clearly this feature is not taught or suggested by Ramanath.

Indeed, the Examiner attempts to equate the silicon substrate 8, the self-assembled monolayer diffusion barrier layer 7 and the copper layer 6 with the template, the semiconductor material and the self-assembled connection of the claimed invention, respectively. This is completely unreasonable.

In fact, as illustrated in Figure 1 of Ramanath, the diffusion barrier (e.g., layer 4 in Figure 1) is formed on the silicon layer 1, and copper dots 5 are formed on the diffusion barrier 4. Ramanath explains that the diffusion barrier "serves to inhibit diffusion of a deposited metal on the surface of the self-assembled monolayer through to the substrate underneath the monolayer" (Ramanath at [0047]). Thus, the function of the diffusion barrier in Ramanath is completely different from the semiconductor material in the claimed invention.

Moreover, nowhere does Ramanath even teach or suggest that the diffusion barrier is "semiconductor". Indeed, it certainly is not important in Ramanath whether the diffusion barrier is semiconductor, since the diffusion barrier is simply intended to inhibit diffusion. Therefore, it is completely unreasonable to equate the diffusion barrier in Ramanath with the semiconductor material of the claimed invention.

Further, as noted above, Ramanath simply teaches that the copper layer (e.g., copper dots 5) are simply formed on the diffusion barrier (e.g., diffusion barrier 4). That is, nowhere

does Ramanath teach or suggest that the copper layer is formed between a semiconductor material and a second layer of a template. Therefore, it is completely unreasonable for the Examiner to equate the copper layer 6 of Ramanath with the self-assembled connection of the claimed invention.

Thus, Ramanath clearly does not teach or suggest a circuit including a template including first and second layers, a semiconductor material self-assembled on a side of the first layer of the template, and a self-assembled connection between the semiconductor material and the second layer of the template, as in the claimed invention.

Therefore, Applicant submits that Ramanath does not teach or suggest each and every feature of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

On page 2 of the Office Action, the Examiner has requested non-patent literature cited "on page 7 and page 8 of the current specification". Applicant presumes that the Examiner is referring to Hermanson et al., "Dielectrophoretic Assembly of Electrically Functional Microwires from Nanoparticle Suspensions", *Science*, Vol. 294, p. 1082 (2001) and C. D. Dimitrakopoulos and P. R. L. Malenfant, *Advanced Materials*, V. 14, p. 99, 2002 which are referenced on pages 7 and 9 of the Application, respectfully. Applicant notes that he is in the process of preparing an IDS for submitting these articles and will file the IDS shortly.

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: November 19, 2008

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